WHAT IS CLAIMED

1. A method for controllably asserting a clock signal on a clock signal bus of an integrated circuit comprising the steps of:

in the absence of a first clock signal being coupled to a prescribed conductor of said integrated circuit, coupling a second clock signal as a default clock signal to said clock signal bus of said integrated circuit; and

in response to said first clock signal being coupled to said prescribed conductor of said integrated circuit, interrupting the coupling of said second clock signal to said clock signal bus of said integrated circuit and, in place thereof, coupling said first clock signal to said clock signal bus of said integrated circuit.

2. The method according to claim 1, further including the steps of:

storing electrical energy in an electrical storage device;

controlling the energy storage state of said electrical storage device in accordance with whether or not said first clock signal is coupled to said prescribed conductor of said integrated circuit, and

controllably coupling one of said first clock signal and said second clock signal to said clock signal bus, in accordance with the energy storage state of said electrical

storage device.

3. The method according to claim 2, wherein said electrical energy storage device comprises a capacitor which stores electrical energy provided by way of a current source coupled thereto.

4. The method according to claim 3, wherein the step of controlling the energy storage state of said electrical storage device comprises repeatedly discharging said capacitor in accordance with said first clock signal, but otherwise allowing said capacitor to be charged.

5. The method according to claim 4, wherein the step of interrupting the coupling of said second clock signal to said clock signal bus of said integrated circuit comprises causing said first clock signal to be coupled to said clock signal bus, in response to a voltage developed across said capacitor being less than a predetermined reference voltage.

6. The method according to claim 5, wherein the step of controlling the energy storage state of said electrical storage device comprises generating a delayed version of first external clock signal and controllably discharging said capacitor in accordance with a prescribed logical relationship between said first clock signal and said

delayed version of said first clock signal.

7. A circuit for controllably asserting either an internal clock signal or an external clock signal on a clock signal bus of an integrated circuit comprising:

an internal clock signal transport path that is operative, in the absence of said external clock signal being coupled to a prescribed conductor of said integrated circuit, to couple said internal clock signal as a default clock signal to said clock signal bus of said integrated circuit; and

an external clock signal transport path that is operative, in response to said external clock signal being coupled to said prescribed conductor of said integrated circuit, to interrupt the coupling of said internal clock signal to said clock signal bus of said integrated circuit in and, in place thereof, to couple said external clock signal to said clock signal bus of said integrated circuit.

8. The circuit according to claim 7, further including:

an electrical storage device which stores electrical energy supplied thereto;

a discharge control circuit which is operative to control the energy storage state of said electrical storage device in accordance with whether or not said external clock signal is coupled to said prescribed conductor of

said integrated circuit, and wherein

said internal and external clock signal transport paths are operative to controllably couple one of said external clock signal and said internal clock signal to said clock signal bus, in accordance with the energy storage state of said electrical storage device.

9. The circuit according to claim 8, wherein said electrical energy storage device comprises a capacitor which stores electrical energy provided by way of a current source coupled thereto.

10. The circuit according to claim 9, wherein said discharge control circuit is operative to repeatedly discharge said capacitor in accordance with said external clock signal, but otherwise allow said capacitor to be charged.

11. The circuit according to claim 10, wherein said external clock signal transport path is operative to cause said external clock signal to be coupled to said clock signal bus, in response to a voltage developed across said capacitor being less than a predetermined reference voltage.

12. The circuit according to claim 11, wherein said discharge control circuit is operative to generate a

delayed version of external clock signal and controllably discharge said capacitor in accordance with a prescribed logical relationship between said external clock signal and said delayed version of said external clock signal.

13. A clock signal generator that is exclusive of a clock selection pin comprising a multiplexer having a first input to which an external clock signal is applied and a second input to which an internal clock signal is applied, said external clock signal being further coupled to an inverting delay and to a first input of a logic circuit, the output of said inverting delay being coupled to a second input of said logic circuit, said logic circuit having an output thereof coupled to a control input of a switching device, said switching device having a current flow path coupled to a current source and in parallel with a capacitor, and wherein a common connection between said current source and said electrical energy storage device is coupled to a first input of a comparator, said comparator having a second input coupled to receive a reference voltage, and an output coupled to a select port of said multiplexer, and wherein said switching device is operative to repeatedly discharge the capacitor in accordance with said external clock signal, but to otherwise allow the capacitor to be charged by the current source, so that said external clock signal is coupled to the output of said multiplexer, as long as the capacitor is repeatedly

discharged by said external clock signal at a frequency sufficient to maintain the voltage across said capacitor less than a prescribed reference voltage.

14. The clock signal generator according to claim 13, wherein said electrical energy storage device comprises a capacitor which stores electrical energy provided by way of a current source coupled thereto.

15. The clock signal generator according to claim 14, wherein said switching device is operative to repeatedly discharge said capacitor in accordance with application of said external clock signal to said first input of said multiplexer, but to otherwise allow said capacitor to be charged by said current source.